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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/784,587	02/15/2001	Matthew D. Kirkwood	00-488 (4028-00200)	5657

24319 7590 11/10/2003

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EXAMINER	
PATEL, NIMESH G	

ART UNIT	PAPER NUMBER
2189	4

DATE MAILED: 11/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/784,587	KIRKWOOD, MATTHEW D.	
	Examiner	Art Unit	
	Nimesh G Patel	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-20* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 February 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 5 recites the limitation "the HBUSREQ signal" in line 2 of the claim. There is insufficient antecedent basis for this limitation in the claim.

3. Claim 6 recites the limitation "the HBUSGRANT signal" in line 2 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Lo et al.(6,425,071) hereinafter referred to as Lo('071).

6. Regarding claim 1, Lo('071) discloses an ASIC comprising of an internal bus operating at first clock frequency and a bridge coupling signals from the internal bus to an off-chip device operating at a second clock frequency(Column 2, Lines 20-23, Column 3, Lines 66-67, and Column 4, Lines 1-2). Therefore claim 1 is rejected.

7. Regarding claim 17, Lo('071) discloses an ASIC comprising of an internal bus operating at first clock frequency and means for coupling signals from the internal bus to an off-chip device operating at a second clock frequency(Column 2, Lines 20-23, Column 3, Lines 66-67, and Column 4, Lines 1-2). Therefore claim 17 is rejected.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 2, 3, 7, 9-16, and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo('071), Lo et. al(6,366,97) hereinafter referred to as Lo('973), and AMBA specification version 2.0 in view of Hofmann et al.(6,633,994) hereinafter referred to as Hofmann.

10. Regarding claim 2, Lo('071) discloses a Wait signal that is used to insert wait cycles until a data transfer is complete(Column 4, Lines 20-22). Lo('973) further discloses in patent '973, which is incorporated by reference in the Lo('071) patent, registers storing and coupling data between an internal bus and an off-chip device(Column 3, Lines 12-13).

Lo does not specifically mention modifying a HREADY signal. However the HREADY signal is a defined signal in the AMBA specification Version 2.0(Section 3.3) that is also used to insert wait cycles until a data transfer is complete. Therefore it is

obvious to use the HREADY signal to insert wait cycles since wait cycles will be needed for the two buses with different frequencies to handle data transfers properly.

Lo does not specifically disclose a clock divider. However, Hofmann discloses circuitry that receives a first frequency and outputs clock cycle control data at second frequency(Column 4, Lines 45-52). It would have been obvious to combine the teachings of Hofmann with Lo's system since it would allow the two buses to communicate at the appropriate frequency.

11. .Regarding claim 3, Hofmann discloses a configuration register storing a variable identifying a second frequency(Column 4, Lines 49-52).

12. Regarding claim 7, Lo does not specifically mention storing addresses assigned to the off-chip device.

However, AMBA specification Version 2.0 discloses addresses stored in registers(Section 3.8). Therefore it would have been obvious to use registers to store addresses assigned to the off-chip device since the correct read and write operations can be performed on the off-chip device.

13. Regarding claim 9, Lo('973) discloses a method for coupling signals from an internal bus to an off-chip device comprising of loading data into registers and then transferring the data to the off-chip device(Column 3, Lines 28-53).

Lo does not specifically disclose the write cycle. However, AMBA specification discloses a method for detecting the start of a bus write cycle and comparing the address signal to addresses assigned to the slave devices, and holding the HREADY signal low until data transfer is complete(Section 3.4, and Section 3.8). Therefore, it

would have been obvious to use the AMBA specification to handle write operations since this would insure the proper operation of the bus.

14. Regarding claim 10, the HREADY signal is a defined signal in the AMBA specification Version 2.0(Section 3.3) that is used to indicate when date transfer is complete. Therefore it would have been obvious to assert the HREADY signal on the internal bus since this would indicate a device is ready and the internal bus can proceed with the next operation.

15. Regarding claim 11, the AMBA specification Version 2.0 discloses addresses for the off-chip device being stored in registers(Section 3.8).

16. Regarding claim 12, Lo('071) discloses an ASIC comprising of an internal bus operating at first clock frequency and a bridge coupling signals from the internal bus to an off-chip device operating at a second clock frequency(Column 2, Lines 20-23, Column 3, Lines 66-67, and Column 4, Lines 1-2).

Lo does not disclose a register for storing a variable identifying the difference between the first and second frequencies nor a clock divider. However, Hofmann discloses circuitry that detects the clock ratio and stores it in registers. Hofmann further discloses circuitry that receives a first frequency and outputs clock cycle control data at second frequency(Column 4, Lines 45-52). It would have been obvious to combine the teachings of Hofmann with Lo's system since it would allow the two buses to communicate at the appropriate frequency.

17. Regarding claim 13, Lo('973) discloses a method for coupling signals from an internal bus to an off-chip device comprising of loading data into registers and then transferring the data to the internal bus(Column 7, Lines 30-64).

Lo does not specifically disclose the read cycle. However, the AMBA specification discloses a method for detecting the start of a bus read cycle and comparing the address signal to addresses assigned to the slave devices, and holding the HREADY signal low until data transfer is complete(Section 3.4, and Section 3.8). Therefore, it would have been obvious to use the AMBA specification to handle read operations since this would insure the proper operation of the bus.

18. Regarding claim 14, the HREADY signal is a defined signal in the AMBA specification Version 2.0(Section 3.3) that used to signify when a device is ready for data transfer. Therefore it would have been obvious to assert the HREADY signal on the internal bus since this would indicate a device is ready and the internal bus can proceed with the next operation.

19. Regarding claim 15, the AMBA specification Version 2.0 discloses addresses for the off-chip device being stored in registers(Section 3.8).

20. Regarding claim 16, Lo('071) discloses an ASIC comprising of an internal bus operating at first clock frequency and a bridge coupling signals from the internal bus to an off-chip device operating at a second clock frequency(Column 2, Lines 20-23, Column 3, Lines 66-67, and Column 4, Lines 1-2).

Lo does not disclose a register for storing a variable identifying the difference between the first and second frequencies nor a clock divider. However, Hofmann

discloses circuitry that detects the clock ratio and stores it in registers. Hofmann further discloses circuitry that receives a first frequency and outputs clock cycle control data at second frequency(Column 4, Lines 45-52). It would have been obvious to combine the teachings of Hofmann with Lo's system since it would allow the two buses to communicate at the appropriate frequency.

21. Regarding claim 18, Lo does not specifically disclose a clock divider. However, Hofmann discloses circuitry that receives a first frequency and outputs clock cycle control data at second frequency(Column 4, Lines 45-52). It would have been obvious to combine the teachings of Hofmann with Lo's system since it would allow the two buses to communicate at the appropriate frequency.

22. Regarding claim 19, Hofmann discloses registers storing clock cycle data(Column 4, Lines 45-53).

23. Regarding claim 20, Lo('973) discloses circuitry for storing and coupling data between an internal bus and an off-chip device(Column 3, Lines 28-53, Column 7, Lines 30-64).

Lo does not specifically mention modifying a HREADY signal. However the HREADY signal is a defined signal in the AMBA specification Version 2.0(Section 3.3) that is also used indicate when date transfer is complete. Therefore it is obvious to use the HREADY since it would allow the two buses with different frequencies to handle data transfers properly.

24. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lo and further in view of Kost(6,535,018).

Regarding claim 8, Lo does not specifically mention devices operating at different voltage levels. However, Kost discloses devices operating at first and second voltage levels, further comprising input output buffers converting signals from first and second voltage levels(Column 1, Lines 45-54). Therefore it would have been obvious to use the teachings of Kost in Lo's system because it would allow a device to interface with a broad range of input/output devices, which may be required to support various potential user-defined applications.

Allowable Subject Matter

25. Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

26. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Lo et al.(6,247,082) discloses a method and circuit for providing handshaking to transact information across mutiple clock domains,

Reiss et al.(6,571,308) discloses a circuit for bridging a host bus to an external bus using a host-bus-to-processor protocol translator.

Pontius et al.(6,467,010) discloses a method and arrangement for passing data between a reference chip and an external bus.

Reis et al.(5,734,877) discloses a processor chip having on-chip circuitry for generating a programmable clock signal for controlling data.

Lai et al.(6,079,027 and 6,709,027) discloses a computer chip set for a motherboard referencing various clock rates.

Jacobs(5,909,563) discloses a computer system with an interface for transferring data between two clock domains.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nimesh G Patel whose telephone number is 703-305-7583. The examiner can normally be reached on M-F, 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-2100.

Nimesh G Patel
Examiner
Art Unit 2189

NGP
11/4/03

Glenn A. Auve
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